REMARKS/ARGUMENTS

Amendments were made to the specification to correct errors and to clarify the specification. No new matter has been added by any of the amendments to the specification.

Claims 1-24 are pending in the present application. With this amendment, claims 1-3, 5-7, 9-11, 13-15, and 17-24 were amended. Reconsideration of the claims is respectfully requested.

I. Interview

Applicants appreciate the courtesies extended by the Examiner and his Supervisor during the interview that was held on August 4, 2006. The translation of Japanese Patent Application Publication 11-205353 was discussed. Neither Applicants' specification nor Applicants' claims were discussed; therefore, no agreement was reached regarding the patentability of Applicants' claims.

II. Oath/Declaration

The Examiner stated that the oath/declaration is defective because non-initialed and/or non-dated alterations have been made to it. Applicants intend to file an amended Declaration that is in compliance with 37 C.F.R. 1.67(a).

III. 35 U.S.C. § 101

The Examiner has rejected claims 17-24 under 35 U.S.C. § 101 as being directed towards non-statutory subject matter. The Examiner stated that the specification described transmission-type media that are not deemed to fall within a statutory category of invention. Applicants have amended the specification to remove the language that described transmission-type media. Therefore, this rejection has been overcome and should be withdrawn.

IV. 35 U.S.C. § 112, First Paragraph

The Examiner has rejected claims 1-24 under 35 U.S.C. § 112, first paragraph, as failing to comply with the written description requirement. Specifically, the Examiner stated that the specification and claim recite processing hardware reset requests without using the queue.

Applicants have amended the claims and the specification to remove the phrases regarding processing the hardware reset requests without utilizing the queue. No new matter has been added. A few typographical errors have been corrected. The specification and the claims now consistently describe the hardware reset requests being processed using the queue.

This rejection has been overcome by the amendments to the specification and the claims and should be withdrawn.

V. 35 U.S.C. § 112, Second Paragraph

The Examiner has rejected claims 1-24 under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicants regards as the invention. Applicants have amended the claims and believe this rejection has been overcome by these amendments and should be withdrawn.

Claims 1, 9, and 17 have been amended to remove the phrase regarding the hardware reset requests being processed without using the queue.

Claims 2, 10, and 18 have been amended to correct the antecedent basis. The claims now describe a plurality of resource cards that include the second resource card, which is recited in the respective independent claims.

Claims 3, 11, and 19 have been amended to correct the antecedent basis of the phrase "a serial order".

Claims 5, 13, and 21 have been amended to describe "in response to determining" which now refers to the feature of determining whether all of said plurality of resource cards have completed servicing of any pending sequence of multiple software communication requests, which is recited in an earlier respective parent claim.

Claims 17-24 have been amended to describe each instruction means as being separate instruction means.

VI. 35 U.S.C. § 103, Obviousness

The Examiner has rejected claims 1-24 under 35 U.S.C. § 103 as being unpatentable over Applicants' Admitted Prior Art (hereinafter *AAPA*) in view of Japanese Patent Application Publication No. 11-205353 (hereinafter *Kuriyama*). This rejection, as it might be applied to the claims as amended, is respectfully traversed.

Applicants' independent claims describe similar features. Claim 1, which is representative of these claims, describes a method in a computer system for serializing hardware reset requests in a software communication request queue in a processor card. The processor card processes software requests utilizing the queue in a serial order. The computer system includes the processor card and a second resource card. A hardware reset request that requests the processor card to reset the second resource card is received within the processor card from an application. The hardware reset request is placed in the queue that is included in the processor card. Requests from the queue are processed in the

serial order. The hardware reset request is processed when all requests from the queue currently being serviced have completed being serviced. The processor card resets the second resource card in response to the hardware reset request being processed.

Applicants' Admitted Prior Art (*AAPA*) does not teach a hardware reset request, a hardware reset request from an application that requests the processor card to reset the second resource card, a hardware reset request that requests the processor card to reset the second resource card that is received within the processor card, placing a hardware reset request in the queue, processing a hardware reset request when all requests from the queue currently being serviced have completed being serviced, or the processor card resetting the second resource card in response to the hardware reset request being processed.

AAPA does not teach a "hardware reset request". *AAPA* teaches a service processor generating a hardware reset through a hardware reset line in order to reset a microcontroller. *AAPA* also teaches the hardware reset, which is not a software communication request, pulling the hardware reset line high which triggers a reset in every resource card that is coupled to the reset line. See Applicants' specification page 2, lines 1-16. Applicants do not describe the hardware reset that the service processor generates as being a "hardware reset request".

Furthermore, while a "request" can be placed in a queue, the actual reset itself of the hardware cannot be placed in a queue. Applicants do not claim placing the actual reset of the hardware in a queue. Applicants claim placing a hardware reset request in a queue. Therefore, it is clear that *AAPA* does not teach a hardware reset request.

AAPA does not teach a hardware reset request that requests the processor card to reset the second resource card. Applicants claim a hardware reset request that is received from an application. *AAPA* teaches a service processor generating a hardware reset that pulls a hardware reset line high but is silent as to what caused the service processor to generate this reset. *AAPA* does not teach the service processor pulling the line high in response to a receipt of a request. *AAPA* does not teach the service processor pulling the line high in response to a hardware reset request that is received from a software application. Teaching the service processor generating a hardware reset does not teach a hardware reset request that requests the processor card to reset the second resource card.

AAPA does not teach a hardware reset request that is received within the processor card. *AAPA* does not teach a hardware reset request; therefore, *AAPA* does not teach a hardware reset request that is received within a processor card.

AAPA does not teach placing a hardware reset request in a queue. *AAPA* does not teach a hardware reset request; therefore, *AAPA* does not teach placing a hardware reset request in a queue.

AAPA does not teach processing a hardware reset request when all requests from a queue currently being serviced have completed being serviced. *AAPA* does not teach a hardware reset request;

therefore, *AAPA* does not teach processing a hardware reset request when all requests from a queue currently being serviced have completed being serviced.

AAPA does not teach the processor card resetting the second resource card in response to the hardware reset request being processed. *AAPA* teaches the service processor generating a hardware reset, which is not a hardware reset request. *AAPA* teaches the hardware reset pulling the hardware reset line high which triggers a reset in every resource card that is coupled to the reset line, but does not describe what caused the service processor to generate the hardware reset. The service processor generating a hardware reset does not teach the processor card resetting the second resource card in response to the hardware reset request being processed. *AAPA* does not teach the processor card resetting the second resource card in response to a hardware reset request being processed.

Kuriyama also does not teach the features of Applicants' claims. *Kuriyama* teaches a first node in a network that is coupled to a second node in the network using a bus. When a node processes a bus reset signal, the node performs tree discernment and bus discernment. The tree discernment and bus discernment processes identify the connection relationships of the nodes connected by the bus.

When a new node is coupled to the first node, the first node generates a bus reset signal and transmits it to the second node. When the second node receives the bus reset signal, the second node postpones its processing of the bus reset signal until a packet is received that indicates all nodes have finished their isochronism data communications.

Applicants' claims describe a computer system that includes a processor card and a second processor card. *Kuriyama* does not teach a computer system that includes a processor card and a second processor card. *Kuriyama* teaches a plurality of nodes where each node is an AV device, such as a computer. See paragraph 2.

Applicants describe a queue and a processor card that includes a queue. Applicants claim placing a hardware reset request in the queue that is included in the processor card. *Kuriyama* does not teach a queue. *Kuriyama* does not teach a processor card that includes a queue. The Examiner states that *Kuriyama* teaches waiting for the current data transfers to complete and that this has the same function as a queue. Applicants disagree. Waiting for the current data transfers to complete does not teach a queue, and does not teach a processor card that includes a queue.

Applicants claim a hardware reset request that requests the processor card to reset the second resource card being received within the processor card from an application. *Kuriyama* does not describe a hardware reset request that requests the processor card to reset the second processor card.

The bus reset signal of *Kuriyama* is transmitted from a first node to a second node. The bus reset signal does not request the first node to reset the second node. In fact, a first node does not reset a second node in *Kuriyama*.

When a node processes a bus reset signal, the node performs self/tree discernment. These discernment processes identify the connection relationships of the nodes. Identifying connection relationships is not a reset of the node; therefore, *Kuriyama* does not teach any kind of node reset.

Furthermore, *Kuriyama* does not teach a request that requests a first node to reset a second node. The bus reset signal is not a request that requests a first node to perform any kind of action on the second node. The bus reset signal is merely an indication to the second node that the second node should enter a particular state; an indication that a node should enter a particular state is not a request that a first node perform an action on the second node.

Applicants claim placing a hardware reset request in the queue that is included in the processor card. *Kuriyama* does not teach placing a hardware reset request in a queue that is included in a processor card. *Kuriyama* does not teach a queue; therefore, *Kuriyama* does not teach placing anything in a queue, and certainly does not teach placing a hardware request in a queue. Furthermore, *Kuriyama* does not teach placing a hardware reset request in the queue that is included in the processor card.

Applicants claim processing requests from the queue in the serial order, and the hardware reset request being processed when all requests from the queue currently being serviced have completed being serviced. *Kuriyama* does not teach either a queue or a hardware reset request; therefore, *Kuriyama* does not teach processing requests from the queue in the serial order, and a hardware reset request being processed when all requests from the queue currently being serviced have completed being serviced.

Applicants claim the processor card resetting the second resource card in response to the hardware reset request being processed. As discussed above, *Kuriyama* does not teach one node resetting another node. *Kuriyama* does not teach a hardware reset request. Therefore, *Kuriyama* does not teach a processor card resetting the second resource card in response to the hardware reset request being processed.

Because neither *AAPA* nor *Kuriyama* teaches the features of Applicants' claims, the combination of *AAPA* and *Kuriyama* does not teach or suggest the features of Applicants' claims.

VII. Conclusion

It is respectfully urged that the subject application is patentable over the combination of *AAPA* and *Kuriyama* and is now in condition for allowance.

The Examiner is invited to call the undersigned at the below-listed telephone number if in the opinion of the Examiner such a telephone conference would expedite or aid the prosecution and examination of this application.

DATE: August 15, 2006

Respectfully submitted,

/Lisa L.B. Yociss/

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